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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| EXAMINER | |
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| AFTERGUT, JEFF H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1733 | |

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/616,341 | DAY ET AL. | |
| | Examiner | Art Unit | |
| | Jeff H. Aftergut | 1733 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 and 3-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

***Claim Rejections - 35 USC § 103***

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1, 3-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Admitted Prior Art in view of Japanese Patent 2000-68620 and Gerber et al (all newly cited).

The admitted prior art as characterized on pages 1-2 of the specification made it clear that in the formation of printed wiring boards it was known at the time the invention was made to form the same via a laminating operation which included the step of roughening the entire surface of the substrates to be laminated with the dielectric material in order to provide adequate adhesion between the copper and the dielectric in the laminated structure. Typically prior to the lamination operation the surfaces of the substrates are smooth and they are roughened along their entire surface in order to promote adhesion. The conventional known techniques for roughening the surface prior to the lamination operation included oxide and oxide replacement processes as well as the application of brass, zinc, or nickel onto the copper surface. Thus, it was known prior to lamination to roughen the surface of the substrate including the copper over the entirety of the surface of the substrate and that prior to the roughening operation the substrate surfaces were known to have been smooth. The admitted prior art failed to teach the selective roughening of the signal plane which did not include all of the signal plane but rather included the lands on the surface of the same and that the lamination

operation was performed with a sticker sheet (a dielectric film or ply formed from epoxy and fiberglass material, i.e. a prepreg for example).

However, in order to facilitate the formation of fine lines in the circuit pattern of a substrate in a printed circuit board, it was known at the time the invention was made to roughen only the surface of the land regions where the through holes were to be formed and to not roughen the other areas of the copper layer of the assembly as such allowed for formation of a fine circuit patterns in the copper foil as evidenced by Japanese Patent '620. The reference to Japanese Patent '620 additionally suggested that the roughening of the substrate at the land regions resulted in better conductive contact at the through hole regions. Applicant is more specifically referred to paragraphs [0011]-[0012] and [0065]. Note that the regions of the lands of the copper layer 3 are roughened where the through hole was to be formed while the other regions of the copper layer 3 were not roughened. It should be noted that copper layers 3 were disposed adjacent each other with a dielectric material 1 disposed there between. The references failed to expressly teach that it was known to employ a sticker sheet in the lamination of the layers together in the manufacture of the circuit board.

The reference to Gerber clearly expressed that it was known at the time the invention was made to employ a sticker sheet to join the conductive substrates together wherein the sticker sheet was formed from a dielectric material. More specifically, Gerber suggested that it was known to apply an adhesive film 58, 24, 60, and 62 to join the layers of the multilayer board together. The reference suggested that the adhesive was in the form of a film layer, see the abstract of the disclosure and column 5, lines 44-

46 for example and additionally suggested that the adhesive layers were electrically insulative, see column 5, lines 44-46, column 5, lines 58-63. Clearly, the use of an adhesive sticker sheet which was a dielectric adhesive layer was known to assembly of plural layers in the lamination of a multilayer printed circuit board. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply a sticker sheet to join plural layers of a multilayer assembly of a circuit board formed via lamination as suggested by Gerber (note that the admitted prior art suggested that the boards were formed via lamination and Gerber is just evidencing that which was conventionally known at the time the invention was made as a suitable manner for lamination of the layers together in a multilayer board) wherein one only roughened the surface of the lands of the copper foil of the substrate where a through hole was to be formed as such would have allowed for finer circuit patterns in the remainder of the copper layer as suggested by Japanese Patent 2000-68620 in the process of making a multilayer circuit board as taught by the applicant's admitted prior art.

With regard to claims 3-5, 8, and 9, the applicant is advised that the admitted prior art appears to suggest that the surfaces of the layers are smooth having a roughness of less than 1 $R_z$ when no roughening operation was performed and that in the typical roughening operation of the prior art the roughness appeared to have been greater than 3 $R_z$. the roughening of the surface appears to have been to promote better adhesion of the layers and one would have understood that roughness greater than 3 $R_z$ would have provided for the same. Additionally the reference to Japanese Patent '620 clearly roughened the surface in order to ensure a tight assembly at the land region

which was subjected to through hole formation. The specific degree of roughening would have been determined through routine experimentation and would have included use of the conventional roughening techniques (the same techniques employed by applicant) in order to provide adequate contact of the plies as well as avoidance of roughness in those regions where fine circuitry was desired in accordance with Japanese Patent '620. Regarding claims 6 and 7, the applicant is advised that the reference suggested that there were several lands which were roughened in each layer of the assembly, see the Figures of the reference wherein the surfaces included at least three lands. Additionally, note that the reference suggested that adjacent layers would have been roughened in order to facilitate joinder in the land region. The use of roughening of both the signal layer and the voltage plane in only selective regions therein would have been understood in light of the teachings of the reference to Japanese Patent '620 to have been performed in the processing therein. With respect to claims 10-15, one skilled in the art would have understood how to utilize a mask to prevent roughening in those regions where it was undesirable. Additionally, the specified roughening techniques of plating and or oxide or an oxide replacement process were known to those skilled in the art at the time the invention was made and admitted by applicant as known for the purpose of roughening the layer in circuit board manufacture. The specific manner that one roughened the surface is taken as well known in the art and additionally the use of a photoresist in the operation is likewise taken as conventional in the art. One skilled in the art would have been expected to

utilize the known techniques for roughening in order to perform the selective roughening of the substrate as taught by Japanese Patent '620.

***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 12, 13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 12, line 2, the applicant refers to the "signal plane" as the surface being treated and then on line 3 recites that it is the "voltage plane" which is being treated. This is confusing. It is suggested that "voltage" on line 3 of claim 12 be changed to --signal--.

In claim 13, line 1, the applicant has amended the claim to recite that the claim depends from claim 10 rather than claim 8, however claim 8 is the first claim which recited that both the voltage plane and the signal plane were roughened in order to provide for the second roughness for both layers. It is suggested to provide proper antecedent basis for the recited language of the claim that claim 13 be made dependent upon claim 8 rather than claim 10.

In claim 15, line 2, the applicant has amended the claim to recite that the signal plane is the surface being treated but has not amended line 3 of the claim which refers to the voltage plane as the surface being treated. It is suggested that "voltage" on line 3 of claim 15 be changed to --signal--.

***Response to Arguments***

5. Applicant's arguments with respect to claims 1 and 3-15 have been considered but are moot in view of the new ground(s) of rejection.

The applicant argues that the prior art failed to teach the selective roughening of the signal plane whereby not all of the signal plane was roughened but at least the land regions were roughened. The reference to Japanese Patent '620, newly cited, clearly suggested only roughening the land regions in order to make a circuit layer which has fine circuitry thereon. Additionally, it would appear from a reading of the background of the invention that the improvement provided by applicant was this selective roughening. The reference to Japanese Patent '620 provided motivation as to why one skilled in the art would have provided only selective roughening for the surface (to allow for finer circuitry to be provided for on the layer).

The applicant is advised that while the reference did not expressly recite the roughness values: (1) the prior art applied suggested that one skilled in the art would have utilized the same roughening techniques; (2) the prior art suggested that roughening in the land region was desirous to provide stronger bond in the region of the through hole, and; (3) the prior art non-roughened surfaces were recited as "smooth" in the disclosure and the roughened surfaces of the admitted prior art were roughened for facilitating a bond (thus one skilled in the art would have determined through routine experimentation the degree of roughening of the surface in order to obtain an adequate bond and such would have included the specified roughness values recited).

Regarding the specific techniques used to roughen, these are taken as conventional in the art. Additionally the use of a mask and/or photoresist in the roughening operation is likewise taken as conventional in the art of circuit board manufacture.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff H. Aftergut whose telephone number is 571-272-1212. The examiner can normally be reached on Monday-Friday 7:15-345 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff H. Aftergut
Primary Examiner
Art Unit 1733

JHA
May 17, 2006